# INTRODUCTION TO GPU COMPUTING

Comtegra Workshop Nov 18

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## NAVIGATING TO COURSES

- 1. Navigate to: <u>https://www.nvidia.com/en</u> <u>-us/deep-learning-</u> <u>ai/education/</u>
- 2. Google search for nvidia dli
- 3. Scroll down Training Online ELECTIVES

Use NV Developer login or new account.



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### **GPU CPU DIFFERENCES**

### Accelerated Computing CPU/GPU differences

10x Performance & 5x Energy Efficiency for HPC



## Accelerated Computing

10x Performance & 5x Energy Efficiency for HPC

### CPU Optimized for Serial Tasks



### CPU Strengths

#### Optimized for

- Very large main memory
- Very fast clock speeds
- Latency optimized via large caches
- Small number of threads can run very quickly

**CPU** Weaknesses

- Relatively low memory bandwidth
- Cache misses very costly
- Low performance/watt



## Accelerated Computing

10x Performance & 5x Energy Efficiency for HPC

### **GPU** Strengths

- High bandwidth main memory
- Significantly more compute resources
- Latency tolerant via parallelism
- High throughput
- High performance/watt

#### GPU Weaknesses

- Relatively low memory capacity
- Low per-thread performance

### **GPU Accelerator**

Optimized for Parallel Tasks







### **Accelerator Nodes**



RAN

CPU and GPU have distinct memories

- CPU generally larger and slower
- GPU generally smaller and faster

### CPU and GPU communicate via PCIe

- Data must be copied between these memories over PCIe
- PCIe Bandwidth is much lower than either memories

## LOW LATENCY OR HIGH THROUGHPUT?

CPU architecture must minimize latency within each thread GPU architecture hides latency with computation from other thread warps



## Some Terminology



- Kernel A function which runs on the GPU
  - A kernel is launched on a grid of thread blocks.
  - The grid and block size are called the launch configuration.
- Global Memory GPU's on-board DRAM
- Shared Memory On-chip fast memory local to a thread block

## SIMT Execution Model



### Software

# **C** Thread







Hardware





Threads are executed by CUDA Cores

Thread blocks are executed on multiprocessors

Thread blocks do not migrate

Several concurrent thread blocks can reside on one multiprocessor - limited by multiprocessor resources (shared memory and register file)

A kernel is launched as a grid of thread blocks





## **HELLO WORLD!**

## Hello World!



```
int main(void) {
    printf("Hello World!\n");
    return 0;
}
```

- Standard C that runs on the host
- NVIDIA compiler (nvcc) can be used to compile programs with no *device* code

Output:

\$ nvcc hello\_world.cu \$ a.out Hello World! \$

### Hello World! with Device Code



```
global void mykernel(void) {
}
```

```
int main(void) {
    mykernel<<<1,1>>>();
    cudaDeviceSynchronize();
    printf("Hello World!\n");
    return 0;
}
```

Two new syntactic elements...

## Hello World! with Device Code



\_\_global\_\_ void mykernel(void) {
}

CUDA C/C++ keyword \_\_global\_\_ indicates a function that:

- Runs on the device
- Is called from host code

nvcc separates source code into host and device components

- Device functions (e.g. mykernel()) processed by NVIDIA compiler
- Host functions (e.g. main()) processed by standard host compiler
  - gcc, cl.exe

### Hello World! with Device Code



mykernel<<<1,1>>>();

Triple angle brackets mark a call from host code to device code

- Also called a "kernel launch"
- We'll return to the parameters (1,1) in a moment
- That's all that is required to execute a function on the GPU!





## RUNNING IN PARALLEL BLOCKS & THREADS

## **IDs and Dimensions**



### Built-in variables:

- threadIdx.[x y z]
  - thread index within a thread block
- blockIdx.[x y z]
  - block index within the grid.
- blockDim.[x y z]
  - Number of threads in each block.
- gridDim.[x y z]
  - Number of blocks in the grid.

Device				
Grid	l			
	Block (0,0,0)	Block (1,0,0)	Block (2,0,0)	
	Block (0,1,0)	Block (1,1,0)	Block (2,1,0)	
i i		N. Contraction	The second se	
Block	x (1,1,0)			

Thread	Thread	Thread	Thread	Thread
(0,0,0)	(1,0,0)	(2,0,0)	(3,0,0)	(4,0,0)
Thread	Thread	Thread	Thread	Thread
(0,1,0)	(1,1,0)	(2,1,0)	(3,1,0)	(4,1,0)
Thread	Thread	Thread	Thread	Thread
(0,2,0)	(1,2,0)	(2,2,0)	(3,2,0)	(4,2,0)

## Parallel Programming in CUDA C/C++

- But wait... GPU computing is about massive parallelism!
- We need a more interesting example...
- We'll start by adding two integers and build up to vector addition





## Vector Add: GPU's Hello World



- GPU is parallel computation oriented.
  - Vector add is a very simple parallel algorithm.
- Problem: C = A + B
  - C, A, B are length N vectors

```
void vecAdd(int n, float * a,
                                 float * b, float * c)
{
    for(int i=0; i<n; i++)
    {
        c[i] = a[i] + b[i];
    }
}</pre>
```

## Vector Add: GPU's Hello World



### GPU is parallel computation oriented.

Vector add is a very simple parallel algorithm.

Problem: C = A + B

C, A, B are length N vectors

```
void vecAdd(int n, float * a,
                                float * b, float * c)
{
    for(int i=0; i<n; i++)
    {
        c[i] = a[i] + b[i];
    }
}</pre>
```

```
void main()
```

```
int N = 1024;
float * a, *b, *c;
a = (float*)malloc(N*sizeof(float));
b = (float*)malloc(N*sizeof(float));
c = (float*)malloc(N*sizeof(float));
memset(c, 0, N*sizeof(float));
init_rand_f(a, N);
init_rand_f(b, N);
```

```
vecAdd(N, a, b, c);
```

## **Moving Computation to the GPU**



### Step 1: Identify parallelism.

- Design problem decomposition
- Step 2: Write your GPU Kernel
- Step 3: Setup the Problem
- Step 4: Launch the Kernel
- Step 5:Copy results back from GPU

Remember: big font means important

### Parallelization of VecAdd





### Parallelization of VecAdd





### Parallelization of VecAdd





## Indexing Arrays with Blocks and Threads



No longer as simple as using blockIdx.x and threadIdx.x

Consider indexing an array with one element per thread (8 threads/block)



- With blockDim.x threads per block, a unique index for each thread is given by:
  - o int index = blockIdx.x \* blockDim.x + threadIdx.x

## Vector Add: GPU's Hello World





### Step 3: Setup the problem



#### void main()

int N = 1024;float \*a, \*b, \*c; float \*devA, \*devB, \*devC; a = (float\*)malloc(N\*sizeof(float)); b = (float\*)malloc(N\*sizeof(float)); c = (float\*)malloc(N\*sizeof(float)); cudaMalloc(&devA, N\*sizeof(float)); cudaMalloc(&devB, N\*sizeof(float)); cudaMalloc(&devC, N\*sizeof(float));

#### memset(c, 0, N\*sizeof(float)); init rand f(a, N); init rand f(b, N);

cudaMemcpy(devA, a, N\*sizeof(float), cudaMemcpyHostToDevice); cudaMemcpy(devB, b, N\*sizeof(float), cudaMemcpyHostToDevice);

#### Pointers to storage on the GPU.

Allocate memory in the GPU Global Memory.

Copy data to the GPU.

## Step 4: Launch the GPU Kernel





Normal parameter passing syntax. Note that *devA*, *devB*, and *devC* are **device pointers.** They point to memory allocated on the GPU.

## Step 5: Copy data back.



vc {	ld main()	
	· • •	
	<pre>cudaMemcpy(c, devC, N*sizeof(float), cudaMemcpyDeviceToHost);</pre>	
}		

## Handling Arbitrary Vector Sizes



Typical problems are not even multiples of **blockDim.x** Avoid accessing beyond the end of the arrays:

```
__global___void add(int *a, int *b, int *c, int n) {
    int index = blockIdx.x * blockDim.x + threadIdx.x;
    if(index<n)
        c[index] = a[index] + b[index];
}</pre>
```

Update the kernel launch: add <<<(N + M-1) / M, M>>>(a, b, c, N); N = problem size, M = block size

## **Multi-Dimensional Thread-Blocks**

### CUDA supports up to 3-dimensional grids and blocks.

- threadIdx.{x,y,z}
- blockIdx.{x,y,z}
- blockDim.{x,y,z}
- gridDim.{x,y,z}
- Easily accelerate multiple nested loops
- Launch a 2D grid using dim3 structures
  - kernel<<<dim3(32,32),dim3(32,4)>>>()

Order of loops is important for performance. Ideally threadIdx.x is consecutive in memory

for(int y=...) -> int y=blockIdx.y\*blockDim.y+threadIdx.y;
for(int x=...) -> int x =blockIdx.x\*blockDim.x+threadIdx.x;



GPUs do work in parallel







GPU work is done in a thread







Many threads run in parallel







A collection of threads is a **block** 







There are many blocks







A collection of blocks associated with a given kernel launch is a **grid** 



### GPU



Kernels are **launched** with an **execution configuration** 











## **COOPERATING THREADS**





- Consider applying a 1D stencil to a 1D array of elements
  - Each output element is the sum of input elements within a radius
- If radius is 3, then each output element is the sum of 7 input elements:



### **Implementing Within a Block**



Each thread processes one output element

- blockDim.x elements per block
- Input elements are read several times
  - With radius 3, each input element is read seven times

### **Sharing Data Between Threads**



- Terminology: within a block, threads share data via shared memory
- Extremely fast on-chip memory, user-managed
- Declare using <u>shared</u>, allocated per block
- Data is not visible to threads in other blocks

## **Implementing With Shared Memory**



### Cache data in shared memory

- Read (blockDim.x + 2 \* radius) input elements from global memory to shared memory
- Compute blockDim.x output elements
- Write blockDim.x output elements to global memory
- Each block needs a halo of radius elements at each boundary







### void \_\_syncthreads();

### Synchronizes all threads within a block

Used to prevent RAW / WAR / WAW hazards

### All threads must reach the barrier

In conditional code, the condition must be uniform across the block

### **Stencil Kernel**



```
global _____void stencil_ld(int *in, int *out) {
    ____shared____int temp[BLOCK_SIZE + 2 * RADIUS];
    int gindex = threadIdx.x + blockIdx.x * blockDim.x;
    int lindex = threadIdx.x + radius;
```

```
// Read input elements into shared memory
temp[lindex] = in[gindex];
if (threadIdx.x < RADIUS) {
   temp[lindex - RADIUS] = in[gindex - RADIUS];
   temp[lindex + BLOCK_SIZE] = in[gindex + BLOCK_SIZE];
}</pre>
```

// Synchronize (ensure all the data is available)
\_\_\_\_syncthreads();

### **Stencil Kernel**

}



```
// Apply the stencil
int result = 0;
for (int offset = -RADIUS ; offset <= RADIUS ; offset++)
    result += temp[lindex + offset];</pre>
```

// Store the result
out[gindex] = result;





# **MANAGING THE DEVICE**

### **Coordinating Host & Device**



- Kernel launches are asynchronous
  - Control returns to the CPU immediately

### CPU needs to synchronize before consuming the results

cudaMemcpy()Blocks the CPU until the copy is complete<br/>Copy begins when all preceding CUDA calls have completedcudaMemcpyAsync()Asynchronous, does not block the CPUcudaDeviceSynchronize()Blocks the CPU until all preceding CUDA calls have completed

## **Reporting Errors**



All CUDA API calls return an error code (cudaError\_t)

- Error in the API call itself OR
- Error in an earlier asynchronous operation (e.g. kernel)

### Get the error code for the last error:

cudaError\_t cudaGetLastError(void)

Get a string to describe the error:

char \*cudaGetErrorString(cudaError\_t)

printf("%s\n", cudaGetErrorString(cudaGetLastError()));

### **Device Management**



### Application can query and select GPUs

cudaGetDeviceCount(int \*count)
cudaSetDevice(int device)
cudaGetDevice(int \*device)
cudaGetDeviceProperties(cudaDeviceProp \*prop, int device)

Multiple threads can share a device

A single thread can manage multiple devices cudaSetDevice(i) to select current device cudaMemcpy(...) for peer-to-peer copies<sup>+</sup>



### **EXECUTION CONFIGURATION**

### **Blocks Size Guidelines**



Block size cannot be larger than 1024 threads

Block size = blockDim.x \* blockDim.y \* blockDim.z

### For performance

- Block size should be divisible by 32
- Have at least 128 threads per block

### • Tip:

start with 128 threads per block and tune up by increments of 32 if necessary

### GV100 Compute Capability 7.0



GPU	Kepler GK180	Maxwell GM200	Pascal GP100	Volta GV100
Compute Capability	3.5	5.2	6.0	7.0
Threads / Warp	32	32	32	32
Max Warps / SM	64	64	64	64
Max Threads / SM	2048	2048	2048	2048
Max Thread Blocks / SM	16	32	32	32
Max 32-bit Registers / SM	65536	65536	65536	65536
Max Registers / Block	65536	32768	65536	65536
Max Registers / Thread	255	255	255	255*
Max Thread Block Size	1024	1024	1024	1024
FP32 Cores / SM	192	128	64	64
# of Registers to FP32 Cores Ratio	341	512	1024	1024
Shared Memory Size / SM	16 KB/32 KB/48 KB	96 KB	64 KB	Configurable up to 96 KB

Compute Capabilities and SM limits of comparable Kepler, Maxwell, Pascal and Volta GPUs. (\*The per-thread program counter (PC) that forms part of the improved SIMT model typically requires two of the register slots per thread.)

### **Occupancy Calculator**





 $occupancy = \frac{blocks \ per \ SM \times threads \ per \ block}{maximum \ threads \ per \ SM}$ 

- Occupancy calculator shows trade-offs between thread count, register use, shared memory use
- Low occupancy is bad
  - Increasing occupancy doesn't always help

### JUPYTER NOTEBOOK

Key components are the grey boxes, that are executable cells. This is where you will be able to modify codes or use a command line.

The executable boxes are those that have "IN []:" in front of the box. The blank space between brackets means that it hasn't been run yet, and to run it you have to click in the box and press the play button (see below). Or you may also hit Control + Enter.





### JUPYTER NOTEBOOK

Once it is successfully running, you will see a number appear, such as the order as they have been executed.

In [1]: print "The answer should be three: " + str(1+2)

The answer should be three: 3

Let's execute the cell below to display information about the GPUs running on the server.

In [ ]: !nvidia-smi

Introduction



