

ACCELERATED COMPUTING: THE PATH FORWARD

Gunter Roeth, Senior Solution Architect

Agenda

9h30 -10h00 Introduction 10h00 - 10h30 ONTAP 10h30 -12h00 GPU Programming Guide 12h00 12h10 Coffee Break 12h10 - 14h10 Hands-On 14h10-14h40 Lunch 14h40 -15h40 Deep Learning SDK (cuDNN, TensorRT, DL Frameworks) 15h40- 15h50 Coffee Break 15h50-17h50 Image Classification with DIGITS (Hands-On) 17h50-18h00 Wrap up and Q&A

NAVIGATING TO COURSES

- 1. Navigate to: <u>www.nvidia.co.uk/dlilabs</u>
- 2. Google search for nvidia dli
- 3. Scroll down Training Online ELECTIVES

Use NV Developer login or new account.

Accelerating Applications with CUDA C/C++



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INTRODUCTION

NVIDIA

- Founded in 1993
- ➢ HQ in Santa Clara
- > Jensen Huang, Founder & CEO
- ➢ 11,000 employees
- > \$9.7B in FY18



Computer Graphics

GPU Computing

Artificial Intelligence

ACCELERATED COMPUTING

Performance & Energy Efficiency

HIGH PERFORMANCE COMPUTE AI / DEEP LEARNING Image: A in the init of th

DATA ANALYTICS



ACCELERATED VDI



NVIDIA TESLA PLATFORM

World's Leading Data Center Platform for Accelerating HPC and AI



CONTINUED DEMAND FOR COMPUTE POWER

Ever-increasing compute power Demand in HPC

Neural Network complexity is Exploding



Comprehensive Earth System Model



Simulation of combustion for new high-efficiency, lowemision engines.



Coupled simulation of entire cells



Predictive calculations for supernovae



NVIDIA POWERS WORLD'S FASTEST SUPERCOMPUTER

Summit Becomes First System To Scale The 100 Petaflops Milestone





27,648 Volta Tensor Core GPUs

GPUS FOR HPC AND DEEP LEARNING

Huge demand on compute power (FLOPS)

NVIDIA Tesla V100



5120 energy efficient cores + TensorCores 7.8 TF Double Precision (fp64), 15.6 TF Single Precision (fp32) , 125 Tensor TFLOP/s mixed-precision

Huge demand on communication and memory bandwidth

CoWoS with HBM2



900 GB/s Memory Bandwidth Unifying Compute & Memory in Single Package

NVLink



6 links per GPU a 50 GB/s bi-

directional for maximum

scalability between GPU's

NCCL



High-performance multi-GPU and multi-node collective communication primitives optimized for NVIDIA GPUs

GPU Direct / GPU Direct RDMA



Direct communication between GPUs by eliminating the CPU from the critical path

NEW VOLTA SM MICROARCHITECTURE

TESLA V100

21B transistors 815 mm²

80 SM 5120 CUDA Cores 640 Tensor Cores

16/32 GB HBM2 900 GB/s HBM2 300 GB/s NVLink



VOLTA GV100 SM

Redesigned for Productivity

Completely new ISA Twice the schedulers Simplified Issue Logic Large, fast L1 cache Improved SIMT model Tensor acceleration

	GP100	GV100
FP32 units	64	64
FP64 units	32	32
INT32 units	NA	64
Tensor Cores	NA	8
Register File	256 KB	256 KB
Unified L1/Shared memory	L1: 24KB Shared: 64KB	128 KB
Active Threads	2048	2048

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VOLTA TENSOR CORE

TENSOR CORE

Mixed Precision Matrix Math - 4x4 matrices

New CUDA TensorOp instructions & data formats

4x4x4 matrix processing array

D[FP32] = A[FP16] * B[FP16] + C[FP32]

Using Tensor cores via

- Volta optimized frameworks and libraries (cuDNN, CuBLAS, TensorRT, ..)
- CUDA C++ Warp Level Matrix Operations





CUBLAS GEMMS FOR DEEP LEARNING

V100 Tensor Cores + CUDA 9: over 9x Faster Matrix-Matrix Multiply



Note: pre-production Tesla V100 and pre-release CUDA 9. CUDA 8 GA release.



UNIFIED MEMORY

Large datasets, simple programming, High Performance



STATE OF UNIFIED MEMORY

High performance, low effort





Performance vs no Unified Memory

PGI OpenACC on Pascal P100

Geometric mean across all 15 SPEC ACCEL™ benchmarks

86% PCI-E, 91% NVLink

PGI 17.1 Compilers OpenACC SPEC ACCEL™ 1.1 performance measured March, 2017. SPEC® and the bendermation name SPEC ACCEL™ are registered trademarks of the Standard Performance Evaluation Corporation.

VOLTA + UNIFIED MEMORY





VOLTA NVLINK

- 6 NVLINKS @ 50 GB/s bidirectional
- Reduce number of lanes for lightly loaded link (Power savings)
- Coherence features for NVLINK enabled CPUs



V100

V100

V100

P9

P9

V100

V100

V100

Hybrid cube mesh (eg. DGX1V)



TESLA GPUS

V100 WITH 16 OR 32GB HBM2

Maintain Form Factor Compatibility

Form Factor		
Performance	7.8T F DP, 15.7 TF SP, 125TF TensorCore	7.0 TF DP, 14.0 TF SP, 112 TF TensorCore
Memory Size	16 or 32GB HBM2	16 or 32GB HBM2
Memory Bandwidth	900GB/s	900GB/s
GPU Peer to Peer	NVLink	PCIe Gen3
Power	300W	250W
Available From All Major OEMs	Hewlett Packard Enterprise	





2,560 CUDA cores + 320 Tensor Cores 8.1 TFLOPS FP32 | 65 FP16 TFLOPS 130 INT8 TOPS | 260 INT4 TOPS

16GB GDDR6 Memory | 320GB/s

75 W Low Profile PCI-e



TESLA PRODUCTS DECODER

	P100 (SXM2)	P100 (PCIE)	P40	P4	T4	V100 (PCIE)	V100 (SXM2)	V100 (FHHL)
GPU CHIP	GP100	GP100	GP102	GP104	TU104	GV100	GV100	GV100
PEAK FP64 (TFLOPs)	5.3	4.7	NA	NA	NA	7	7.8	6.5
PEAK FP32 (TFLOPs)	10.6	9.3	12	5.5	8.1	14	15.7	13
PEAK FP16 (TFLOPs)	21.2	18.7	NA	NA	65	112	125	105
PEAK TOPs	NA	NA	47	22	260	NA	NA	NA
Memory Size	16 GB HBM2	16/12 GB HBM2	24 GB GDDR5	8 GB GDDR5	16 GB HBM2	32 GB HBM2	32 GB HBM2	16GB HBM2
Memory BW	732 GB/s	732/549 GB/s	346 GB/s	192 GB/s	320GB/s	900 GB/s	900 GB/s	900 GB/s
Interconnect	NVLINK + PCIe Gen3	PCIe Gen3	PCIe Gen3	PCIe Gen3	PCIe Gen3	PCIe Gen3	NVLINK + PCIe Gen3	PCIe Gen3
ECC	Internal + HBM2	Internal + HBM2	GDDR5	GDDR5	GDDR6	Internal + HBM2	Internal + HBM2	Internal + HBM2
Form Factor	SXM2	PCIE Dual Slot	PCIE Dual Slot	PCIE LP	PCIE LP	PCIE Dual Slot	SXM2	PCIE Single Slot Full Height Half Length
Power	300 W	250 W	250 W	50-75 W	75 W	250W	300W	150W

DGX-STATION / DGX-1 DGX-2 / HGX-2

NVIDIA DGX-STATION

Al supercomputer for the desk

4x Tesla V100 connected via NVLINK (60 TFLOPS FP32, 0.5 PFLOPS Tensor performance)

Xeon CPU, 256 GB Memory

Storage:

3X 1.92 TB SSD RAID 0 (Data) 1X 1.92 TB SSD (OS)

Dual 10GbE

1500W, Water-cooled \rightarrow Quiet

Optimized Deep Learning Software across the entire stack

Containerized frameworks

Always up-to-date via the cloud





NVIDIA DGX-1

Al supercomputer-appliance-in-a-box

8x Tesla V100 connected via NVLINK (125 TFLOPS FP32, 1 PFLOPS Tensor Core performance)

Dual Xeon CPU, 512 GB Memory

7 TB SSD Deep Learning Cache

Dual 10GbE, Quad IB 100Gb

3RU - 3200W

Optimized Deep Learning Software across the entire stack

Containerized frameworks

Always up-to-date via the cloud





NVIDIA DGX-2



NVSWITCH



- 18 NVLINK ports
 - @50 GB/s per port bi-directional
 - 900 GB/s total bi-directional
- Fully connected crossbar
- X4 PCIe Gen2 Management port
- GPIO
- I2C
- 2 billion transistors

FULL NON-BLOCKING BANDWIDTH



FULL 6-WAY POINT-TO-POINT



INDEPENDENT COMMUNICATION



NVSWITCH



16x 32GB Independent Memory Regions



NVLINK PROVIDES

- All-to-all high-bandwidth peer mapping between GPUs
- Full inter-GPU memory interconnect (incl. Atomics)

UNIFIED MEMORY PROVIDES

- Single memory view shared by all GPUs
- Automatic migration of data between GPUs
- User control of data locality
2X HIGHER PERFORMANCE WITH NVSWITCH



2 DGX-1V servers have dual socket Xeon E5 2698v4 Processor. 8 x V100 GPUs. Servers connected via 4X 100Gb IB ports | DGX-2 server has dual-socket Xeon Platinum 8168 Processor. 16 V100 GPUs

GPU PROGRAMMING

HOW GPU ACCELERATION WORKS



HOW TO START WITH GPUS

1	Applications									
2 Libraries	3 Compiler Directives	4 Programming Languages								
Easy to use	Easy to Start	Most Performance								
Most Performance	Portable Code	Most Flexibility								
	OpenACC	CUDA								

- 1. Review available GPUaccelerated applications
- 2. Check for GPU-Accelerated applications and libraries
- 3. Add OpenACC Directives for quick acceleration results and portability
- 4. Dive into CUDA for highest performance and flexibility

VISION: MAINSTREAM PARALLEL PROGRAMMING

Enable more programmers to write portable parallel software in their language of choice

Embrace and evolve standards in key languages

CUDA continues to evolve as the target low-level platform for GPU acceleration



POPULAR GPU-ACCELERATED APPLICATIONS

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06 Defense and metogence
07 Computational Finance
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Research: Higher Education and Supercomputing

COMPUTATIONAL CHEMISTRY AND BIOLOGY

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Library and application for molecular dynamics for HPC with GP2s

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550+ GPU-Accelerated Applications

www.nvidia.com/appscatalog

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GPU ACCELERATED LIBRARIES

"Drop-in" Acceleration for Your Applications



WHAT IS OPENACC Programming model for an easy onramp to GPUs



Simple

Powerful & Portable

Read more at <u>www.openacc.org/about</u>

OpenACC is an open specification developed by OpenACC.org consortium

Three major concepts

Single Source	Low Learning Curve
	Single Source





Supported Platforms POWER Sunway x86 CPU x86 Xeon Phi NVIDIA GPU PEZY-SC

Single Source

- A single OpenACC code can be compiled for, and ran on, many different parallel hardware
- An OpenACC code retains its ability to run sequentially at all times
- No need for multiple versions of your code

The compiler can be told to **ignore** your OpenACC code additions. This allows you to run the code **sequentially**, regardless of the presence of **OpenACC directives**.

OPENACC IS FOR MULTICORE, MANYCORE & GPUS

98 !\$ACC KERNELS 99 !\$ACC LOOP INDEPENDENT 100 D0 k=y_min-depth,y_max+depth 101 !\$ACC LOOP INDEPENDENT 102 D0 j=1,depth 103 density0(x_min-j,k)=left_density0(left_xmax+1-j,k) 104 ENDDO 105 ENDDO 106 !\$ACC END KERNELS

```
% pgfortran -ta=multicore -fast -Minfo=acc -c \
    update_tile_halo_kernel.f90
```

CPU

```
100, Loop is parallelizable
Generating Multicore code
100, !$acc loop gang102, Loop is parallelizable
```



% pgfortran -ta=tesla,cc35,cc60 -fast -Minfo=acc -c \
 update_tile_halo_kernel.f90

```
100, Loop is parallelizable
```

102, Loop is parallelizable
Accelerator kernel generated
Generating Tesla code
100, !\$acc loop gang, vector(4) ! blockidx%y threadidx%y
102, !\$acc loop gang, vector(32) ! blockidx%x threadidx%x

. . .

SINGLE CODE FOR MULTIPLE PLATFORMS

OpenACC - Performance Portable Programming Model for HPC



Systems: Haswell: 2x16 core Haswell server, four K80s, CentOS 7.2 (perf-hsw10), Broadwell: 2x20 core Broadwell server, eight P100s (dgx1-prd-01), Broadwell server, eight V100s (dgx07), Skylake 2x20 core Xeon Gold server (sky-4).

Compilers: Intel 2018.0.128, PGI 18.1

Benchmark: CloverLeaf v1.3 downloaded from http://uk-mac.github.io/CloverLeaf the week of November 7 2016; CloverLeaf_Serial; CloverLeaf_ref (MPI+OpenMP); CloverLeaf_OpenACC (MPI+OpenACC) NIDIA.

Incremental

- Make small, incremental changes to the code
- If any errors occur, easily able to revert back to an earlier, working version of the code
- Start with a working sequential code, and add improvements

Single Source

- A single OpenACC code can be compiled for, and ran on, many different parallel hardware
- An OpenACC code retains its ability to run sequentially at all times
- No need for multiple versions of your code

Low Learning Curve



The programmer will give hints to the compiler about which parts of the code to parallelize.

The compiler will then generate parallelism for the target parallel hardware.

Low Learning Curve

- OpenACC is meant to be easy to use, and easy to learn
- Supports C, C++, and Fortran coding
- Takes a very high-level approach to parallelism, and allows the compiler to do a lot of extra work in parallelizing the code

Incremental

- Make small, incremental changes to the code
- If any errors occur, easily able to revert back to an earlier, working version of the code
- Start with a working sequential code, and add improvements

Single Source

- A single OpenACC code can be compiled for, and ran on, many different parallel hardware
- An OpenACC code retains its ability to run sequentially at all times
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Low Learning Curve

- OpenACC is meant to be easy to use, and easy to learn
- Supports C, C++, and Fortran coding
- Takes a very high-level approach to parallelism, and allows the compiler to do a lot of extra work in parallelizing the code

OPENACC.ORG RESOURCES

Guides • Talks • Tutorials • Videos • Books • Spec • Code Samples • Teaching Materials • Events • Success Stories • Courses • Slack • Stack Overflow





slack
https://www.openacc.org/community#slack

Resources https://www.openacc.org/resources OpenACC About Tools News Events Re-Resources A complete library of OpenACC materials that includes a collection of video tutorials, guides, online courses, books and more Guides E Book raliel Programming with OpenACC Introduction to OpenACC Quick Guide OpenACC Programming and Best Practices Guid OpenACC 2.5 API Reference Care **Tutorials** gramming Massively Parallel Processors, Third dition: A Hands-on Approach Video tutorials to help start with OpenACC and advance your skills

Compilers and Tools

https://www.openacc.org/tools



Success Stories

https://www.openacc.org/success-stories



Events

https://www.openacc.org/events



Hackathons

Hickshows are the day internite hands-on-mentoring sessions. They are despined to help computational scientists port their applications to GPUs using libraries, OpenCCC, CUDA and other tools. They are currently lead by the O-kink field Leadership Computing Facility (ICCC) at the Oak Redge Netsonical Liboratory (IORL). The the full schedule and registration details please visit <u>https://www.oid.orml.gov/training.com/2012.pps</u>:





PGI – THE NVIDIA HPC SDK

Fortran, C & C++ Compilers Optimizing, SIMD Vectorizing, OpenMP **Accelerated Computing Features OpenACC Directives, CUDA Fortran Multi-Platform Solution** X86-64 and OpenPOWER Multicore CPUs **NVIDIA** Tesla GPUs Supported on Linux, macOS, Windows MPI/OpenMP/OpenACC Tools Debugger **Performance Profiler** Interoperable with DDT, TotalView

PGI[®]

The Compilers & Tools for Supercomputing



PGI COMPILERS FOR EVERYONE

The PGI 18.4 Community Edition

FRE	E		
	PGI ° Community EDITION	Professional EDITION	PGI [°] Enterprise EDITION
PROGRAMMING MODELS OpenACC, CUDA Fortran, OpenMP, C/C++/Fortran Compilers and Tools	\checkmark		
PLATFORMS X86, OpenPOWER, NVIDIA GPU	\checkmark	\checkmark	\checkmark
UPDATES	1-2 times a year	6-9 times a year	6-9 times a year
SUPPORT	User Forums	PGI Support	PGI Premier Services
LICENSE	Annual	Perpetual	Volume/Site

pgicompilers.com/community



CUDA RELEASES

Accelerating the Pace



Four CUDA releases per year

Faster release cadence for new features and improved stability for existing users

Upcoming limited decoupling of display driver and CUDA release for ease of deployment

Monthly cuDNN & other library updates

Rapid innovation in library performance and functionality

Library Meta Packages independent of toolkit for easy deployment



INTRODUCING CUDA 10.0

TURING AND NEW SYSTEMS

New GPU Architecture, Tensor Cores, NVSwitch Fabric



CUDA PLATFORM

CUDA Graphs, Vulkan & DX12 Interop, Warp Matrix





LIBRARIES

GPU-accelerated hybrid JPEG decoding, Symmetric Eigenvalue Solvers, FFT Scaling



DEVELOPER TOOLS

New Nsight Products - Nsight Systems and Nsight Compute

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	MOV R1, c[0x0][0x28];	1	13	4
	\$2R R0, SR_CTAID.X;	2	143	2
	S2R R2, SR_TID.X;	3	0	1
	IMAD R0, R0, c[0x0][0x0], R2;	3	599	9
	ISETP.GE.AND P0, PT, R0, c[0x0]	[ex170] 2	125	
PØ	EXIT;	2	259	
	MOV R2, R0;	3	386	
!PT	SHFL.IDX PT, RZ, RZ, RZ;	2	0	
	MOV 84, 0x4;	3	e	
	IMAD.WIDE R4, R2, R4, c[exe][ex	160]; 4	0	
	LDG.E.SYS R3, [R4];	3	0	
	BSSY 80, 0xb00976780;	3	0	
	SHF.R.S32.HI R0, RZ, 0x1f, R2;	4	•	
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CUDA LIBRARIES

cuFFT 10.0

Multi-GPU Scaling across DGX-2 and HGX-2

- Strong scaling across 16-GPU systems -DGX-2 and HGX-2
- Multi-GPU R2C and C2R support
- Large FFT models across 16-GPUs effective 512GB vs 32GB capacity

Up to 17TF performance on 16-GPUs 3D 1K FFT



cuSOLVER 10.0

Dense Linear Algebra

Improved performance with new implementations for

- Cholesky factorization
- Symmetric & Generalized Symmetric Eigensolver

QR factorization

Up to 44x Faster on Symmetric Eigensolver (DSYEVD)



Benchmarks use 2 x Intel Gold 6140 (Skylake) processors with Intel MKL 2018 and NVIDIA Tesla V100 (Volta) GPUs



CUTLASS

Template library for linear algebra operations in CUDA C++

>90% CUBLAS performance

Open Source (3-clause BSD License) https://github.com/NVIDIA/cutlass





NSIGHT DEVELOPER TOOLS

NSIGHT PRODUCT FAMILY



 GPU Speed of Light 										
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and the second				9.78						
Memory Workload Analysis										
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Scheduler Statistics										
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Nsight Systems

System-wide application algorithm tuning

Nsight Compute

CUDA Kernel Profiling and Debugging

Nsight Graphics

Graphics Shader Profiling and Debugging

IDE Plugins

Nsight Eclipse Edition/Visual Studio (Editor, Debugger)

HIERARCHICAL MEMORY STATISTICS



- -

0 B

160 B

6.368 MiB

14.156 KiB

896.562 MiB

448.25 MiB

L2 Cache

99%

NAVIGATING TO COURSES

- 1. Navigate to: <u>www.nvidia.co.uk/dlilabs</u>
- 2. Google search for nvidia dli
- 3. Scroll down Training Online ELECTIVES

Use NV Developer login or new account.

Accelerating Applications with CUDA C/C++



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DEEP LEARNING SDK

NVIDIA DEEP LEARNING INSTITUTE

Online self-paced labs and instructor-led workshops on deep learning and accelerated computing

Take self-paced labs at www.nvidia.co.uk/dlilabs

View upcoming workshops and request a workshop onsite at www.nvidia.co.uk/dli

Educators can join the University Ambassador Program to teach DLI courses on campus and access resources. Learn more at www.nvidia.com/dli









Fundamentals

Autonomous Vehicles

Healthcare







Digital Content

Intelligent Video Analytics

Robotics



Finance

Accelerated Computing



Virtual Reality

WHY THE EXCITEMENT?

GPUs as Enablers of Breakthrough Results



Paper: H.Zhang et al. StackGAN: Text to Photo-realistic Image Synthesis with Stacked Generative Adversarial Networks, arXiv:1612.03242

WHAT IS DEEP LEARNING?
A NEW COMPUTING MODEL

Algorithms that Learn from Examples



Traditional CV Approach

- Domain experts design feature detectors
- Time consuming
- Quality depends on Algorithms
- Error prone
- Not scalable to new problems
- Need CV experts and time



Deep Learning Approach

- DNN learn from data
- Quality depends on data & training method
- Easily to extend
- Needs lots of <u>data and</u> <u>compute</u>
- Speedup with GPUs

GPUS IN ARTIFICIAL INTELLIGENCE

Machine Learning





IMAGENET

Replace hand-tuned parameters of the feature extraction steps (e.g. in voice and image recognition)

Deep learning is a subset of machine learning that refers to artificial neural networks that are composed of many layers.

Artificial Neural Networks inspired by human brain and need lots of training data (ideal for Big Data).

NVIDIA GPUs and cuDNN software broadly adopted for machine learning.

THE BIG BANG IN MACHINE LEARNING



[#] Google's AI engine also reflects how the world of computer hardware is changing. (It) depends on machines equipped with GPUs... And it depends on these chips more than the larger tech universe realizes."





DEEP LEARNING EVERYWHERE











INTERNET & CLOUD

Image Classification Speech Recognition Language Translation Language Processing Sentiment Analysis Recommendation

MEDICINE & BIOLOGY

Cancer Cell Detection Diabetic Grading Drug Discovery

MEDIA & ENTERTAINMENT

Video Captioning Video Search Real Time Translation

SECURITY & DEFENSE

Face Detection Video Surveillance Satellite Imagery

AUTONOMOUS MACHINES

Pedestrian Detection Lane Tracking Recognize Traffic Sign



ARTIFICIAL NEURONS







TRAINING NEURAL NETWORKS

Find a set of weights that minimizes the misfit.

Error between the target and computed output

 $M(W) = \sum_{i=1}^{Examples} \sum_{j=1}^{Output} (O_{comp \, i,j} - O_{target \, i,j})^2$

Least squares optimization problem

Solution by gradient descent, Monte Carlo, etc.

The gradient can be computed by the backpropagation of the error (delta rule)

$$\delta_{i,j} = g'(I_{i,j})(O_{comp\ i,j} - O_{target\ i,j})$$



DEEP LEARNING APPROACH - TRAINING



Process

- Forward propagation yields an inferred label for each training image
- Loss function used to calculate difference between known label and predicted label for each image
- Weights are adjusted during backward propagation
- Repeat the process



Convolutional Networks Used Case

Local receptive field + weight sharing

Yann LeCun et al, 1998





Laver-1

Input

MNIST: 0.7% error rate

CONVOLUTION



Center element of the kernel is placed over the source pixel. The source pixel is then replaced with a weighted sum of itself and nearby pixels.



CNN TERMINOLOGY





ADDITIONAL TERMINOLOGY

- Hyperparameters parameters specified before training begins
 - Can influence the speed in which learning takes place
 - Can impact the accuracy of the model
 - Examples: Learning rate, decay rate, batch size
- Epoch complete pass through the training dataset
- Activation functions identifies active neurons
 - Examples: Sigmoid, Tanh, ReLU
- Pooling Down-sampling technique
 - No parameters (weights) in pooling layer



DEEP NEURAL NETWORK (DNN)



NVIDIA'S DIGITS

NVIDIA'S DIGITS

Interactive Deep Learning GPU Training System

- Simplifies common deep learning tasks such as:
 - Managing data
 - Designing and training neural networks on multi-GPU systems
 - Monitoring performance in real time with advanced visualizations
- Completely interactive so data scientists can focus on designing and training networks rather than programming and debugging
- Open source



DIGITS - HOME

	1/1 GPU available
er	New Model Images -
mework status elapse	d submitted A
E	er mework status elapse

Click here to see a list of existing datasets or models

Clicking here will present different options for model and dataset creation



DIGITS - DATASET

New Image Classification Dataset

DIGITS New Dataset

DIGITS New Dataset

New Object Detection Dataset

Direct Detection	Dataset Ontions	Image Type 😡		Use Image Folder Use Text Files	
nages can be stored in any of the supported file formats ('png', jpg', jpeg', bmp', ppm').		Color v		Training Images O	
aining image folder 🚱		Image size (Width x Height) 😡		folder or URL	
folder		256 × 25	56	Minimum samples per class 🖗	Maximum samples per cla
abel files are expected to have orresponding label file should fraining label folder 🚱	e the .txt extension. For example if an image file is named foo.png the be foo.txt.	Resize Transformation O		2	
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width	x height		Image Encod	ling 😡	
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RGB	*		Group Name		
linimum box size (in pix	els) for validation set 😡				
25			Dataset Nam	e	
custom classes 🚱					
			Create		
			Create		

Different options will be presented based upon the task



DIGITS - MODEL





EVALUATE THE MODEL





HANDWRITTEN DIGIT RECOGNITION

HELLO WORLD of machine learning?

- MNIST data set of handwritten digits from Yann Lecun's website
- All images are 28x28 grayscale
 - Pixel values from 0 to 255
- 60K training examples / 10K test examples
- Input vector of size 784
 - 28 * 28 = 784
- Output value is integer from 0-9



ADDITIONAL TECHNIQUES TO IMPROVE MODEL

- More training data
- Data augmentation
- Modify the network



ADDITIONAL TERMINOLOGY

- Hyperparameters parameters specified before training begins
 - Can influence the speed in which learning takes place
 - Can impact the accuracy of the model
 - Examples: Learning rate, decay rate, batch size
- Epoch complete pass through the training dataset
- Activation functions identifies active neurons
 - Examples: Sigmoid, Tanh, ReLU
- Pooling Down-sampling technique
 - No parameters (weights) in pooling layer

FIRST RESULTS

Small dataset (10 epochs)

- 96% of accuracy achieved
- Training is done within one minute

	SMALL DATASET
1	1:99.90 %
2	2:69.03%
3	8:71.37 %
4	8:85.07%
17	0:99.00%
8	8:99.69%
8	8:54.75%



SECOND RESULTS

Full dataset (10 epochs)

- 99% of accuracy achieved
- No improvements in recognizing realworld images

	SMALL DATASET	FULL DATASET
1	1:99.90 %	0:93.11%
2	2:69.03 %	2:87.23 %
3	8:71.37 %	8:71.60%
4	8:85.07%	8:79.72%
17	0:99.00%	0:95.82 %
8	8:99.69%	8:100.0%
	8:54.75%	2:70.57 %

DEEP LEARNING

182 🕺

DATA AUGMENTATION

Adding Inverted Images

DIGITS	Image Class	sification Dataset		smorino	(Logout)	Info -	
Explo	Exploring MNIST invert (train_db) images						
Show all im	ages or filter b	oy class: 0 1 2	3 4 5 6 7 8	9			
ltems per p	age: 10 - 25 - 50	- 100					
« 0	1 2 3 4	4 5 360	0 »				
ン	2	9	7	7	3	3	
(4	6		5		
	1	4		6		5	
5	5	3	8	8	8	2	
3	3	1	8	8	6	6	

- Pixel(Inverted) = 255 Pixel(original)
- White letter with black background
 - Black letter with white background
- Training Images: /home/ubuntu/data/train_invert
- Test Image: /home/ubuntu/data/test_invert
 - Dataset Name: MNIST invert



DATA AUGMENTATION

Adding inverted images (10 epochs)

	SMALL DATASET	FULL DATASET	+INVERTED
1	1:99.90 %	0:93.11%	1:90.84 %
2	2:69.03 %	2:87.23 %	2:89.44%
3	8:71.37 %	8:71.60%	3:100.0 %
4	8:85.07 %	8:79.72 %	4:100.0 %
77.	0:99.00 %	0:95.82 %	7:82.84%
8	8:99.69%	8:100.0%	8:100.0%
8	8:54.75%	2:70.57 %	2:96.27%



MODIFY THE NETWORK

Adding filters and ReLU layer

```
layer {
        name: "pool1"
        type: "Pooling"
        ...
}
layer {
        name: "reluP1"
        type: "ReLU"
        bottom: "pool1"
        top: "pool1"
layer {
        name: "reluP1"
```

```
layer {
  name: "conv1"
  type: "Convolution"
         convolution param {
         num output: 75
         . . .
layer {
         name: "conv2"
         type: "Convolution"
         . . .
         convolution param {
         num_output: 100
         . . .
```

185 NIDIA





MODIFIED NETWORK

Adding filters and ReLU layer (10 epochs)

	SMALL DATASET	FULL DATASET	+INVERTED	ADDING LAYER
1	1:99.90 %	0:93.11%	1:90.84 %	1:59.18%
2	2:69.03 %	2:87.23 %	2:89.44%	2:93.39%
3	8:71.37 %	8:71.60%	3:100.0 %	3:100.0 %
4	8:85.07%	8:79.72 %	4:100.0 %	4:100.0%
7	0:99.00%	0:95.82 %	7:82.84 %	2:62.52%
8	8:99.69%	8:100.0%	8:100.0%	8:100.0%
8	8:54.75%	2:70.57 %	2:96.27%	8:70.83%

DEEP LEARNING

187 nvidia

DEEP LEARNING SDK

NVIDIA DEEP LEARNING SOFTWARE PLATFORM



NVIDIA DEEP LEARNING SDK

AI INFERENCING IS EXPLODING



NVIDIA TensorRT

Deep Learning Inference Optimizer and Runtime

High performance neural network inference optimizer and runtime engine for production deployment

Maximize inference throughput for latency-critical services in hyperscale datacenters, embedded, and automotive production environments

Optimize TensorFlow and ONNX-framework models to generate high-performance runtime engines

Deploy faster, more responsive and memory efficient deep learning applications with INT8 and FP16 optimized precision support



NVIDIA TENSORRT 4

RNN and MLP Layers • ONNX Import • NVIDIA DRIVE Support

Maximize RNN and MLP Throughput



Speed up speech, audio and recommender app inference performance through new layers and optimizations Optimize and Deploy ONNX Models

ONNX

Easily import and accelerate inference for ONNX frameworks (PyTorch, Caffe 2, CNTK, MxNet and Chainer)

Support for NVIDIA DRIVE Xavier



Deploy optimized deep learning inference models NVIDIA DRIVE Xavier

Free download to members of NVIDIA Developer Program developer.nvidia.com/tensorrt

DL FRAMEWORKS

NVIDIA Optimized Examples


CONTAINER

CHALLENGES

Current DIY deep learning environments are complex and time consuming to build, test and maintain

Development of frameworks by the community is moving very quickly

Requires high level of expertise to manage driver, library, framework dependencies





SIMPLIFY PORTABILITY WITH NVIDIA CONTAINERS

Benefits of Containers:

Simplify deployment of GPU-accelerated applications

Isolate individual frameworks or applications

Share, collaborate, and test applications across different environments

NVIDIA GPU CLOUD REGISTRY

Common Software stack across NVIDIA GPUs

Deep Learning

All major frameworks with multi-GPU optimizations Uses NCCL for NVLINK data exchange Multi-threaded I/O to feed the GPUs

Caffe, Caffe2, CNTK, mxnet, PyTorch, Tensorflow, Theano, Torch

HPC

NAMD, Gromacs, LAMMPS, GAMESS, Relion, Chroma, MILC

HPC Visualization

Paraview with Optix, Index and Holodeck with OpenGL visualization base on NVIDIA Docker 2.0, IndeX, VMD

Single NGC Account For use on GPUs everywhere - <u>https://ngc.nvidia.com</u>



NVIDIA GPU Cloud containerizes GPUoptimized frameworks, applications, runtimes, libraries, and operating system, available at no charge Container Orchestration for DL Training & Inference



KUBERNETES on NVIDIA GPUs

- Scale-up Thousands of GPUs Instantly
- Self-healing Cluster Orchestration
- GPU Optimized Out-of-the-Box
- Powered by NVIDIA Container Runtime
- Included with Enterprise Support on DGX

CONVERGENCE OF HPC AND AI

INTELLIGENT HPC

DL Driving Future HPC Breakthroughs



- distribute input data
- Control job parameters

- Analyze/reduce/augment output data
- Act on output data

AI Supercomputing is The New computing model

Extending The Reach of HPC By Combining Computational & Data Science



S8242 – DL for Computational Science, Jeff Adie & Yang Juntao Presented ~20 Success Stories of DL in Computational Science (GTC on-demand: http://on-demand-gtc.gputechconf.com)



Al Quantum Breakthrough

Background

Developing a new drug costs \$2.5B and takes 10-15 years. Quantum chemistry (QC) simulations are important to accurately screen millions of potential drugs to a few most promising drug candidates.

Challenge

QC simulation is computationally expensive so researchers use approximations, compromising on accuracy. To screen 10M drug candidates, it takes 5 years to compute on CPUs.

Solution

Researchers at the University of Florida and the University of North Carolina leveraged GPU deep learning to develop ANAKIN-ME, to reproduce molecular energy surfaces with super speed (microseconds versus several minutes), extremely high (DFT) accuracy, and at 1-10/millionths of the cost of current computational methods.

Essentially the DL model is trained to learn Hamiltonian of the Schrodinger equation.

Impact

Faster, more accurate screening at far lower cost





Deep Learning for Computational Physics **DEEP LEARNING FOR GRAVITATIONAL WAVE** DETECTION

Time (sec) Actual Signal Caused by Gravitational Wave

Deep learning method named deep filtering was used in the first detection of gravitational wave. Numerical simulated data was used for training deep filtering, a convolutional neural network to replace matched filtering. It provided 20X speed up on single core and potential to be accelerated further with GPU.









Actual observed data

FEA UPDATED WITH NEURAL NETWORK

FEA trained deep neural network for surrogate modelling of estimated stress distribution. Deepvirtuality, a spinoff from Volkswagen Data:Lab under Nvidia Inception Program has demonstrate with their software aimed for a quicker prediction of structural data.



An demonstration of Structure Born Noise of a V12 Engine with Deepvirtuality

Torsional Frequencies of a Car Body by Deepvirtuallity



https://github.com/uber/horovod, https://eng.uber.com/horovod/

"Horovod is a distributed training framework for TensorFlow. The goal of Horovod is to make distributed Deep Learning fast and easy to use."

Leverage Tensorflow + MPI + NCCL2 for a simplified and performant API to enable synchronous multigpu + multinode Tensorflow.

Instead of Parameter Server architecture leverage MPI.

Support features such as RDMA, GPUDirectRDMA (GDR), via leveraging MPI and NCCL2.

NAVIGATING TO COURSES

- 1. Navigate to: www.nvidia.co.uk/dlilabs
- 2. Google search for nvidia dli
- 3. Scroll down

•Use NV Developer login or new account.

Image Classification with Digits



~ Accelerating Applications with GPU-Accelerated Libraries in Python

x

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NVIDIA DEEP LEARNING INSTITUTE (DLI)

Hands-on training for developers, data scientists, and researchers

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Gunter Roeth (gunterr@nvidia.com)

